Amendments to the Claims

This listing of claims replaces all prior versions and listings of claims:

Listing of Claims:

1. (Currently amended) A solid image capturing element, comprising:

a plurality of vertical shift registers arranged to each correspond to a column of a plurality of light receiving pixels in a matrix arrangement,

a horizontal shift register provided on an output side of the plurality of vertical shift registers, and

an output section provided on an output side of the horizontal shift register,

wherein

~~over one major surface of a semiconductor substrate of one conductive type,~~ a semiconductor region of one conductive type is formed closer to a surface of a semiconductor substrate of one conductive type, while a semiconductor region of reverse conductive type is formed in a deeper portion than the semiconductor region of one conductive type, and a first semiconductor region ~~of an opposite conductive type~~ and a second semiconductor region ~~of the opposite conductive type and~~ having a higher dopant concentration than that of the first semiconductor region are formed in the semiconductor region of reverse conductive type,

the horizontal shift register is formed in the first semiconductor region; and

the output section is formed in the second semiconductor region.

2. (Original) The solid image capturing element according to claim 1, further comprising:

an output gate formed on the semiconductor substrate at a boundary between the horizontal shift register and the output section.

3. (Currently amended) The solid image capturing element according to claim 1, wherein

~~over the one major surface of the semiconductor substrate~~ in the semiconductor region of reverse conductive type, a third semiconductor region ~~of the~~

~~opposite conductive type and~~ having a lower dopant concentration than that of the first semiconductor region is formed, and

~~the plurality of light receiving pixels and~~ the plurality of vertical shift registers are formed in the third semiconductor region.

4. (Currently amended) A method for manufacturing a solid image capturing element having a plurality of vertical shift registers arranged to each correspond to a column of a plurality of light receiving pixels in a matrix arrangement, a horizontal shift register provided on an output side of the plurality of vertical shift registers, and an output section provided on an output side of the horizontal shift register, comprising:

a first step of forming ~~over one major~~ closer to a surface of a conductive semiconductor substrate, a first reverse conductive semiconductor region having a first dopant concentration;

a second step of forming ~~over the one major surface of~~ in a deeper portion in the conductive semiconductor substrate than the conductive semiconductor region, a second reverse conductive semiconductor region having a second dopant concentration which is higher than the first dopant concentration; and

a third step of forming the horizontal shift register on the first reverse conductive semiconductor region and the output section on the second reverse conductive semiconductor region.

5. (Currently amended) The method for manufacturing a solid image capturing element according to claim 4, further comprising:

a fourth step of forming ~~over the one major surface of the conductive semiconductor substrate~~ in the semiconductor region of reverse conductive type, a third reverse, conductive semiconductor region having a third dopant concentration which is lower than the first dopant concentration,

wherein

at the fourth step, the plurality of light receiving pixels and the plurality of vertical shift registers are formed in the third semiconductor region.

6. (Original) The method for manufacturing a solid image capturing element according to claim 4, wherein a dopant is doped in a stepwise manner to the first reverse conductive semiconductor region and the second reverse conductive semiconductor region, and

doping of the dopant is performed commonly at least once to the first reverse conductive semiconductor region, the second reverse conductive semiconductor region, and the third reverse conductive semiconductor region.